Automated Process Metrology in Solar Cell Manufacturing

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***Abstract* — Optimizing a solar cell manufacturing line must take into account a variety of issues. Wafers used for solar cells are typically thinner than those used in semiconductor IC manufacturing. This makes the solar cell wafers susceptible to surface and edge defects such as deep scratches and cracks. The wafer slicing operation can induce thickness non-uniformity as well as surface roughness variation. Wafer texturing (typically via etching) must result in an optimal pyramid height in the case of monocrystalline wafers and an optical grain size in the case of polycrystalline wafers. Silicon Nitride grown on the wafer can induce stress and eventual breakage of the wafer. An uneven nitride film can cause a drop in the overall efficiency of the wafer. The metal contact lines account for a significant cost in the production of a solar cell wafer. The process engineer must pay attention to the contact line height and width while minimizing the total amount of metal used. Based on all these requirements, an optical profiler, the Zeta-200, was developed to provide rapid and meaningful feedback to the process line. In this paper we present results from various process points in solar cell manufacturing, such as bare wafer roughness, silicon nitride film thickness and contact line dimensions.**

I. INTRODUCTION

A key requirement for reducing costs in silicon based solar cells is optimizing the wafer thickness. The thinner the wafer, the more cells can be produced from a given ingot. Wafers are typically sliced using a diamond wire based wafer slicer. Figure 1 shows a typical wafer manufacturing process.

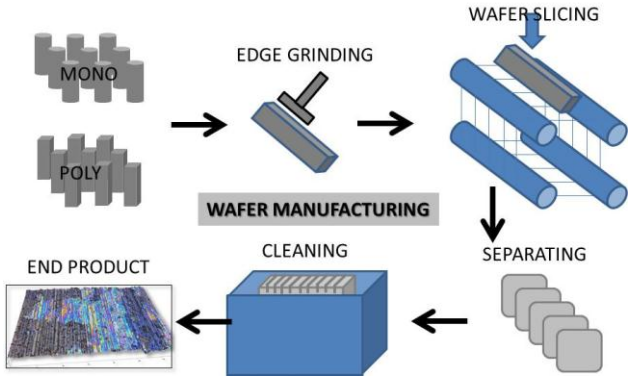

Fig. 1. Silicon wafer production for solar cells.

An ingot (mono or poly) is first cropped at the ends and then sent through a bricking and edge grinding process. It is critical for the edges to be clean and smooth, without any cracks or inclusions that could result in wafer breakage either at the slicing step or at future process steps. The brick is then sent through a wire slicer, which consists of a metal encased wire with diamonds embedded at the surface. At this step it is critical to measure the key machining components, which are the diamond wire and the wire-guide channels in the rollers supporting the wires. Studies have shown that for a given wire, there is a certain number of re-uses beyond which the wire is ineffective in slicing wafers, causing large variations in surface roughness as well as non-uniformity in the wafer thickness across the brick. Other factors such as SiC inclusions caused by carbon precipitation may also cause excessive wear of the diamond wires. As the slicer ages, the channels that serve as wire guides on the rollers start wearing out. This causes the diamond wires to oscillate inside the channels, once again causing variation in wafer surface roughness or wafer thickness or shape (bow). The post clean wafer may have residual stains in case of an improper washing or drying process. The wafers leaving the factory therefore must be inspected for edge defects, surface roughness and overall wafer shape (bow).

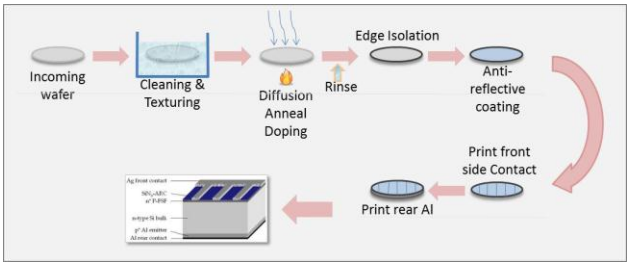

Fig. 2. Crystalline Si solar cell manufacturing process.

Figure 2 shows a typical solar cell manufacturing process. There are a number of process steps critical to the overall yield and end efficiency of the solar cell. The texturing process is critical for generating the correct amount of surface texture. In the case of monocrystalline silicon solar cells, it is vital to monitor the pyramid dimensions and use that as constant feedback to control the etch chemistry as well as the etch time

(Reference 1). Following texturing, the thickness of the anti-reflective coating must be monitored to ensure that the nitride thickness will allow for any surface variations without compromising its ability to protect the silicon surface. The high temperature process may also increase the wafer bow, which may result in wafer breakage at later steps. A significant portion of the manufacturing cost goes into the metals that are used to create the contact lines. However, the contact line has to be thick enough (without breakages) to ensure electrical continuity across the wafer. Therefore, the contact line dimensions must be monitored on a regular basis. Last, but not the least, the overall wafer shape must once again be monitored so that wafers with excessive bow can be eliminated prior to packaging the wafers into a module.

II. EXPERIMENTAL

A Zeta-200 (Figure 3) optical profiler was used to develop metrology solutions for each of the process steps. This non-contact 3D imaging and metrology system incorporates a ZDot™ based vertical scanning mechanism (Figure 4) as well as a wide area Interferometer and Spectroscopic Reflectometer. This flexible architecture enables a multitude of process control measurements mentioned in the previous section. In the ZDot™ mode, the Zeta-200 generates a 3D image of a surface by acquiring a stack of images at various heights, typically a few nanometers apart. Each image is then automatically analyzed to detect the pixels that are in best focus. The height and color of that pixel is recorded. Once all the pixels are accounted for, the system recreates a true color picture of the surface. Unlike a typical vertical scanning microscope, the Zeta-200 incorporates a unique optical design that enables a height resolution of 10nm (as opposed to 700nm on a typical vertical scanning microscope). Special fixtures were developed to scan the diamond wires (about 125µm in diameter). Roller wire- guide channel shapes were imaged by using a soft epoxy to replicate the contour of the wire guide. Another fixture was developed to hold the wafers at a tilted angle and scan the edge (side wall) of the wafer.

Fig. 3. The Zeta-200 optical metrology system.

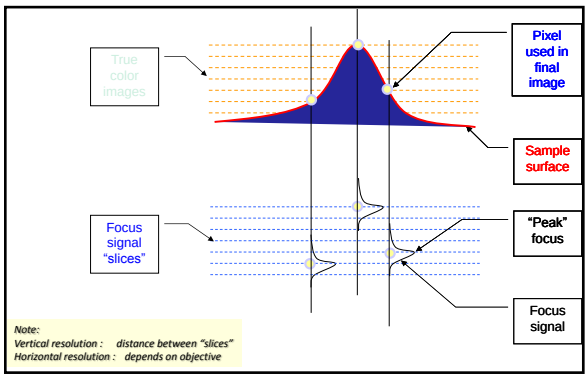

Fig. 4. Vertical scanning and image generation process on the Zeta-200.

III. RESULTS

A. Bare Si Wafer Roughness

Monitoring incoming wafer roughness and shape is critical to ensure that the etch process will result in the desired surface structure (for example, pyramid height in the case of monocrystalline wafers). Large deviations in wafer surface topography may result in non-uniform etching and hence poor cell efficiency at the end of the line. Figure 5(a) shows a wafer with good surface roughness while Figure 5(b) shows a wafer with poor surface roughness. Note that there is a periodicity in both the surface profiles. This comes for the diamond wires oscillating within the wire-guides. However, the wafer shown in Figure 5(b) shows some deep grooves as well. Given the periodic nature of these grooves, they may be the result of unwanted vibration of the diamond wire. Therefore, it becomes important to measure both the diamond wire as well as the wire-guide from time to time.

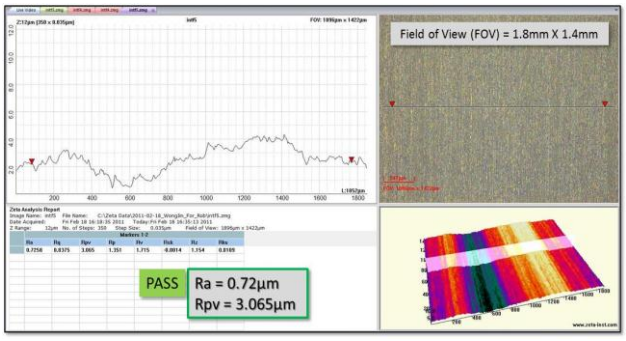

Fig. 5(a). Good wafer quality after slicing.

Fig. 5(b). Bad wafer quality after slicing

B. Wafer Slicing – Diamond Wire

Figure 6 shows the effect of re-using a diamond wire in a wafer slicer. The image on the left shows a new wire which has embedded diamonds that are about 10µm – 12µm tall. The image on the right shows that after reusing the wire multiple times, the diamonds have worn out and are barely 2µm tall. Signs of damage can be observed on the wire. This shows that the wire has to be replaced right away and cannot be re-used, otherwise there will be a significant increase in slicing time as well as a decrease in the wafer surface quality. Monitoring the diamond wire periodically will improve the uptime of the slicer as well as the quality of the wafers. Wire damage can be caused by excessive use, improper force or even Carbon precipitation in the Si boule, which leads to SiC inclusions. SiC inclusions will not only cause wire damage, they will also cause uneven wafer thickness when the wire bends around a inclusion since it cannot pass through it.

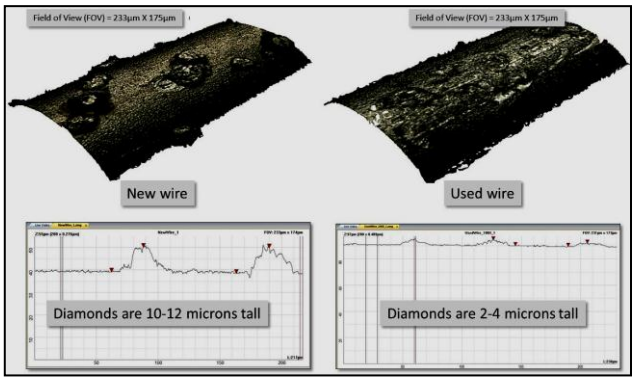

Fig. 6. Monitoring diamond wire quality in wafer slicing operations.

C. Wafer Slicing – Wire Guides

Figure 7 shows the wire guides that carry the diamond wire as it loops around the slicer. Over a period of time, the wire guides start wearing out. This will cause the diamond wire to oscillate during the slicing process, resulting in uneven wafer thickness and surface roughness. Since the wire guides cannot be dismantled to be placed directly on to a profiler, an epoxy (such as Repliset F5 from Struers) can be used to make a replica (negative) of the groove. The epoxy negative can then be placed on the profiler to create a 3D view of the groove.

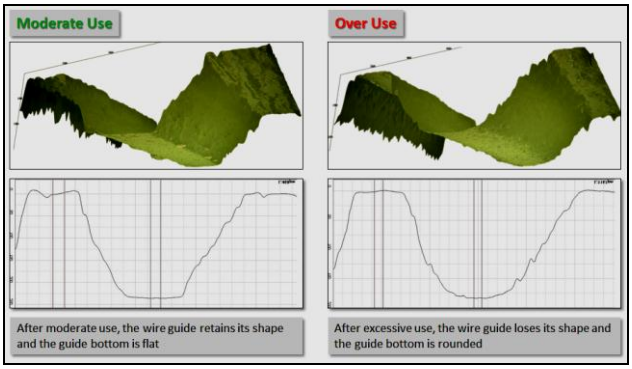

Fig. 7. Monitoring wire guide wear on a wafer slicing machine.

D. Wafer Edge Quality

The edge grinding process is critical to creating a clean wafer edge, without burrs or cracks. Any such defects at the edge of the wafer will result in wafer breakage either during the subsequent processing steps or after the wafer has been integrated into the module. Though it is not possible to inspect 100% of the wafer edge, it is possible to do a quick visual inspection of the edge. Any defects found can be reviewed with a profiler. Figure 8(a) shows the Zeta-200 optical profiler with an edge profiling fixture. This fixture is used to orient the wafers at an angle to enable inspection of the top surface as well as the side wall of the wafer. Figures 8(b) and 8(c) show a wafer with an edge crack and a wafer with good edge quality respectively.

Fig. 8(a). Wafer edge measurement fixture on a Zeta-200 optical profiler.

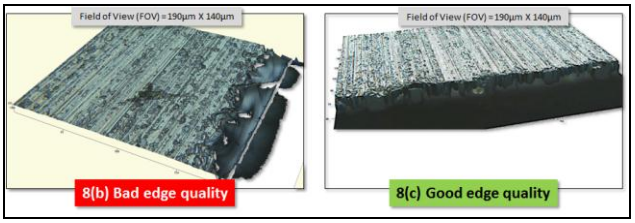

Fig. 8(b) and 8(c). Bad and good wafer edge.

E. Pre-Texture Saw Damage Removal

As seen in the previous sections, variations in the slicing process will damage the surface, causing excessive waviness. This 'saw damage' has to be removed prior to texturing the wafer. Optimal etching of the wafer will remove just enough material, while creating the optimal base size for the next step, which will create the pyramids on the wafer. Figure 9(a) shows a wafer with excessive saw damage removal. The grain dimension on the wafer is roughly 10µm. This will result in a very large pyramid structure on the wafer. Studies have shown that excessively large pyramids reduce the efficiency of the solar cell. Figure 9(b) shows another wafer with an optimal amount of saw damage removal. The approximate grain size in this case is about 5µm. In this case, one can expect an optimal surface area ratio after pyramid texturing.

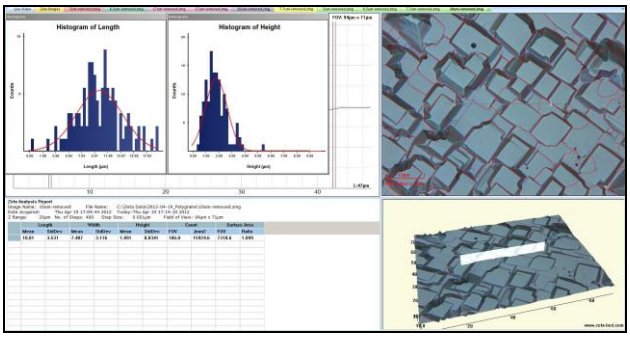

Fig. 9(a). Excessive pre-texture saw damage removal results in large grain sizes (corresponding to a large pyramid base).

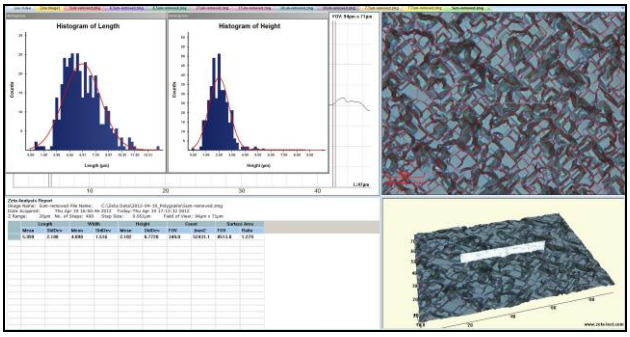

Fig. 9(b). Optimal pre-texture saw damage saw removal (results in the desired pyramid base size).

F. Texture measurements

The pyramids created after the etch process are critical to trapping light and increasing the efficiency of the solar cell. Figure 10 shows an example of textured silicon surface as analyzed by the Zeta-200. Figure 11 shows a textured surface measured after the wafer was coated with Silicon Nitride.

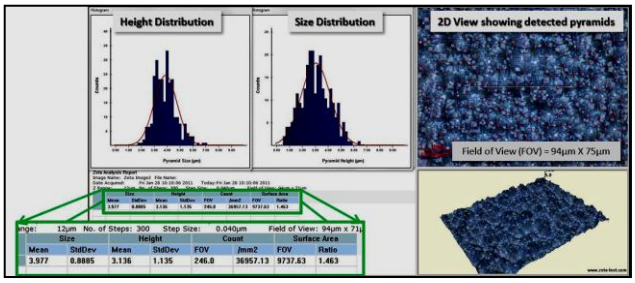

Fig. 10. Automated pyramid texture analysis showing pyramid height and lateral size distribution on a textured silicon wafer

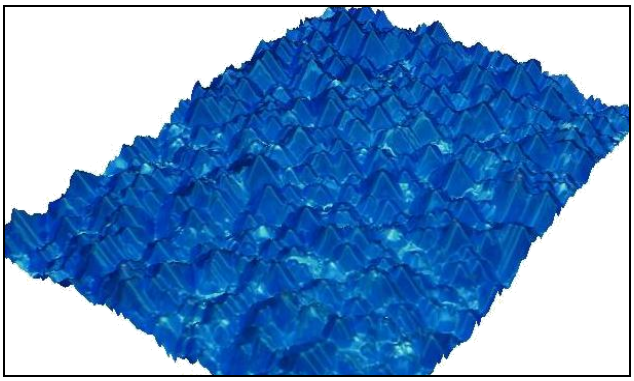

Fig. 11. Textured wafer coated with silicon nitride

Any metrology tool measuring texture should be capable of differentiating between minor changes in pyramid height as well as the lateral size and density. The critical Surface Area Ratio parameter (ratio of actual surface to the projected area plane) should be reported and monitored.

Table 1 shows the analysis of textured wafers supplied by different vendors using different texturing processes. Based on the pyramid texture analysis, the optimal vendor and texture process can be selected to improve the overall yield of the solar cell line.

TABLE 1
TEXTURE HEIGHT DISTRIBUTION OF WAFERS FROM DIFFERENT SOURCES

Batch #	Mean pyramid size, um	Mean pyramid height, um	Surface area ratio
1	5.33	4.12	1.41
2	2.77	1.98	1.15
3	**3.1**	**3.2**	**1.42**
4	4.55	3.75	1.38
5	3.1	2.6	1.31

G. SiN_x Film Thickness Measurement

Following the texturing process, the solar cell wafers are coated with an anti-reflective layer, typically Silicon Nitride. The thickness of this layer is also critical to providing a protective coating to the wafer. The Zeta-200 used in this

study was equipped with a visible light spectroscopic reflectometer. The light reflected from the wafer surface was collected through the objective lens and channeled to a reflectometer via a fiber optic cable. A sequence of 15 sites was automatically scanned using the motorized XY stage on the Zeta-200 and the results are presented in Figure 12. The film thickness values have been overlaid on a picture of the wafer. Reference measurements were acquired on a polished bare Silicon substrate and the thickness of the Silicon Nitride at each location was calculated by fitting a curve to the detected spectrum.

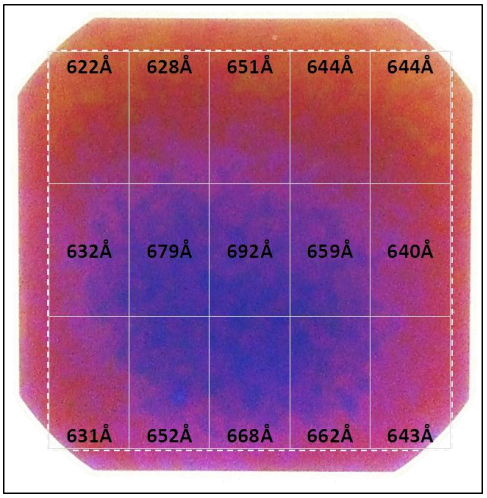

Fig. 12. Monitoring silicon nitride film thickness is important to ensure optimal solar cell performance.

H. Contact Line Dimensions

A major cost of the solar cell is in the metal used to create the contact lines. Screen printing is typically used to create these lines. However, this process is hard to control and as a result the contact lines exhibit a large variation in width and height as they are deposited on the wafers. Figure 13 shows one such contact line. Note that the width as well as the height of the contact line varies by more than 25% within a short distance of 200µm. In such a situation, there will be a significant impact on the electrical performance of the solar cell. A lot of expensive metal is also wasted, resulting in an increased cost of manufacturing the cells.

Inspecting the contact lines requires a non-contact method. The rough nature of the surface as well as the large geometry precludes the use of relatively delicate instruments such as AFMs. Conventional stylus based profilers prove to be too expensive since the rough surface tends to wear down the stylus tips, resulting in tool downtime as well as increased costs of tool maintenance. Optical profilers such as the Zeta-200 used in this study are a good option for this mission critical measurement. Note that the contact line metals have a very high reflectivity (sometimes >90%) whereas the surrounding nitride coated silicon surface has very low reflectivity (typically <0.5%). Therefore, the optical profiler must be capable of handling such a large reflectivity variation in the same field of view. The tool used in this study had two enhancements – a CCD camera with an improved dynamic range, as well as a software algorithm designed to acquire data at various bandwidths and blend it into one continuous image. This enhanced mode, called High Dynamic Range (HDR) enabled the measurement of finger profiles on wafers with less than 0.5% reflectivity in the nitride areas.

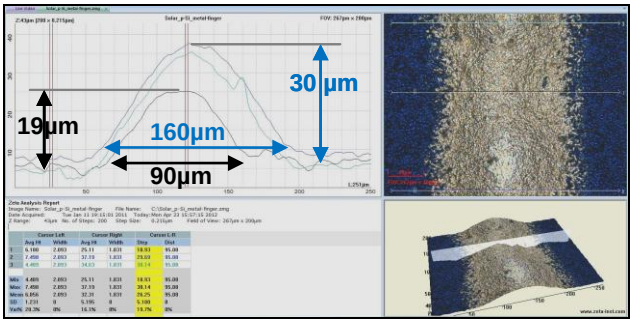

Fig. 13. Typical contact line on a solar cell, exhibiting a large variation in width and height.

Newer methods of contact line deposition are now being developed by leading edge solar cell companies. Figure 14 shows one such contact line which uses significantly less amount of metal. Also note that the height and width of the contact line vary a lot less than the contact line shown in Figure 13. This will enable solar cell manufacturers to save a significant amount of money as well as improve the overall efficiency of the cells. Results from the Zeta-200 were used to develop the process and are being used to monitor the quality of the ongoing production.

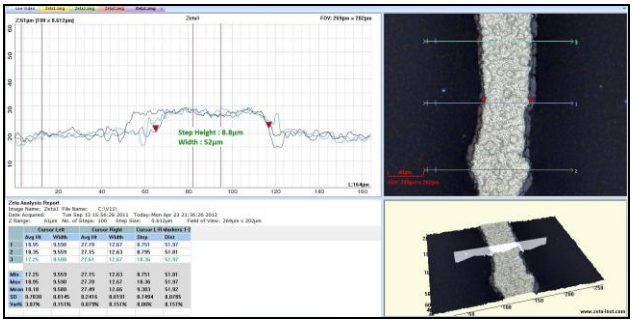

Fig. 14. Newer methods of laying down the metal contact lines enable thinner and more uniform contact lines.

I. Wafer Bow

After the contact lines are printed on the surface, it is important to measure the bow of the wafer prior to incorporating it into the solar cell module. Given that the wafers are typically thinner than 200µm, excessive bow or warpage increases the internal stresses in the wafer and it can lead to cracking or breakage. Figure 15 shows the overall shape of the wafer as measured with a Zeta-200 optical

profiler. A grid of 10X10 data points was used to measure the shape. For quick production monitoring and process development it is enough to take a quick cross-sectional measurement across the wafer. Figure 16 shows the wafer bow as measured across the center on 3 different wafers subjected to 3 different process conditions. The quality of the incoming bare silicon also contributes to the ability of the wafers to withstand stress. Figure 17 shows the bow measured on finished solar cell wafers coming from different wafer vendors. As is evident in the chart, incoming silicon quality can play a major role in reduce wastage due to broken wafers caused by excessive bow.

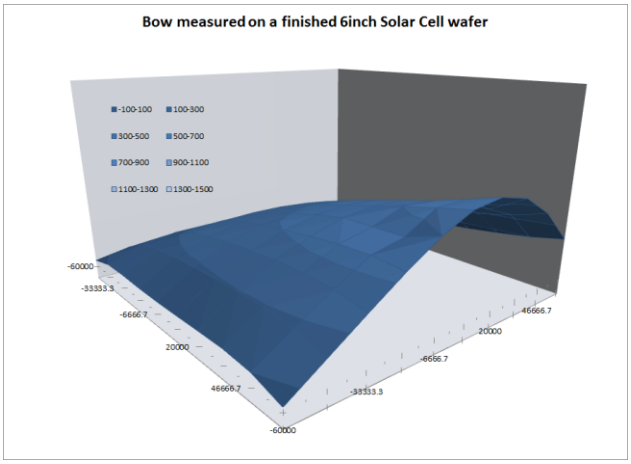

Fig. 15. Overall wafer shape on a 156mm X 156mm wafer after contact line printing.

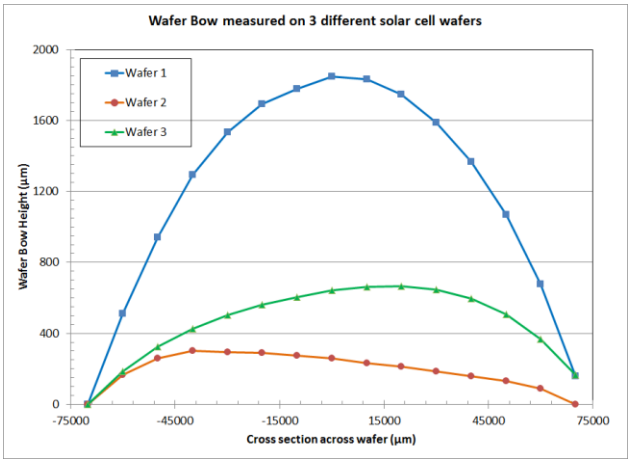

Fig. 16. Wafer bow on 3 different wafers subjected to different process conditions.

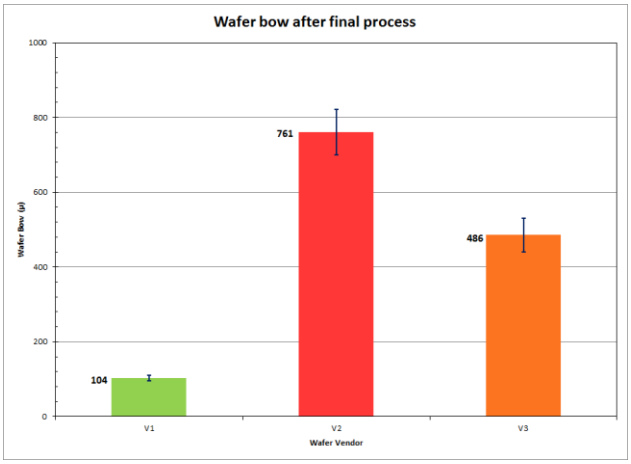

Fig. 17. Variation of wafer bow on wafers from different vendors after contact line printing.

IV. CONCLUSION

As the solar cell industry matures and solar power gains wider adoption, it is important to improve the overall yield of the solar cell manufacturing line. Adopting a metrology strategy that provides critical feedback at various stages will allow for overall yield improvement and reliability of the solar cell modules in the field. Optical profilers offer a good balance between speed and flexibility and therefore can be a good solution for solar cell process control. The optical profiler used in this paper, the Zeta-200, provides critical metrology data at multiple process points in solar cell manufacturing. Wafer roughness, pyramid texture surface parameters, nitride film thickness, wafer bow and contact line dimensions can all be measured via the Zeta-200 optical profiler. The measurements enable the process engineers to qualify various wafer vendors as well as internal processes.

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